

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Previously presented) A method for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 receiving an input signal on a capacitive receiver pad from a capacitive
4 transmitter pad;
5 feeding the input signal through an inverter to produce an output signal;
6 feeding the output signal through a weakened inverter to produce a
7 feedback signal;
8 feeding the feedback signal back into an input of the inverter so as to form
9 a latch for the input signal between the inverter and the weakened inverter; and
10 establishing a high bias voltage, V_H , with a high bias voltage generator and
11 establishing a low bias voltage, V_L , with a low bias voltage generator;
12 wherein the high bias voltage generator includes a mechanism for
13 adjusting the high bias voltage, V_H ;
14 wherein the low bias voltage generator includes a mechanism for adjusting
15 the low bias voltage, V_L ;
16 wherein the weakened inverter is biased to produce the feedback signal
17 that swings between the high bias voltage, V_H , and the low bias voltage, V_L ; and
18 wherein V_H is slightly higher than a switching threshold of the inverter, and
19 V_L is slightly lower than the switching threshold of the inverter, whereby the
20 feedback signal causes the input signal to reside within a narrow voltage range

21 near the switching threshold of the inverter, thereby making the inverter sensitive
22 to small transitions in the input signal received on the capacitive receiver pad.

1 2. (Original) The method of claim 1, further comprising amplifying an
2 output of the inverter through an amplification stage to produce an amplified
3 output signal.

1 3-4 (Canceled).

1 5. (Previously presented) The method of claim 2, further comprising
2 adjusting the high bias voltage generator and the low bias voltage generator to
3 provide a specified sensitivity to transitions of the input signal.

1 6. (Previously presented) The method of claim 2, further comprising
2 adjusting the high bias voltage generator and the low bias voltage generator to
3 provide a specified noise immunity to noise associated with the input signal.

1 7 (Canceled).

1 8. (Previously presented) An apparatus for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 a receiving mechanism configured to receive an input signal on a
4 capacitive receiver pad from a capacitive transmitter pad;
5 a latching mechanism configured to feed the input signal through an
6 inverter to produce an output signal; and
7 a biasing mechanism configured to establishing a high bias voltage, V_H ,
8 with a high bias voltage generator and establishing a low bias voltage, V_L , with a
9 low bias voltage generator;

10 wherein the high bias voltage generator includes a mechanism for
11 adjusting the high bias voltage, V_H ;
12 wherein the low bias voltage generator includes a mechanism for the low
13 bias voltage, V_L ;
14 wherein the latching mechanism is further configured to feed the output
15 signal through a weakened inverter to produce a feedback signal;
16 wherein the latching mechanism is further configured to feed the feedback
17 signal back into an input of the inverter so as to form a latch for the input signal
18 between the inverter and the weakened inverter;
19 wherein the weakened inverter is biased to produce the feedback signal
20 that swings between the high bias voltage, V_H , and the low bias voltage, V_L ; and
21 wherein V_H is slightly higher than a switching threshold of the inverter, and
22 V_L is slightly lower than the switching threshold of the inverter, whereby the
23 feedback signal causes the input signal to reside within a narrow voltage range
24 near the switching threshold of the inverter, thereby making the inverter sensitive
25 to small transitions in the input signal received on the capacitive receiver pad.

1 9. (Original) The apparatus of claim 8, further comprising an amplifying
2 mechanism configured to amplify an output of the inverter through an
3 amplification stage to produce an amplified output signal.

1 10-11 (Canceled).

1 12. (Previously presented) The apparatus of claim 9, further comprising an
2 adjusting mechanism configured to adjust the high bias voltage generator and the
3 low bias voltage generator to provide a specified sensitivity to transitions of the
4 input signal.

1 13. (Previously presented) The apparatus of claim 9, further comprising an
2 adjusting mechanism configured to adjust the high bias voltage generator and the
3 low bias voltage generator to provide a specified noise immunity to noise
4 associated with the input signal.

1 14 (Canceled).

1 15. (Previously presented) A means for latching and amplifying a
2 capacitively coupled inter-chip communication signal, comprising:
3 a receiving means for receiving an input signal on a capacitive receiver
4 pad from a capacitive transmitter pad;
5 a latching means configured to feed the input signal through an inverter to
6 produce an output signal; and
7 a biasing means for establishing a high bias voltage, V_H , with a high bias
8 voltage generator and for establishing a low bias voltage, V_L , with a low bias
9 voltage generator;
10 wherein the high bias voltage generator includes a mechanism for
11 adjusting the high bias voltage, V_H ; and
12 wherein the low bias voltage generator includes a mechanism for the low
13 bias voltage, V_L ;
14 wherein the latching means is further configured to feed the output signal
15 through a weakened inverter to produce a feedback signal;
16 wherein the latching means is further configured to feed the feedback
17 signal back into an input of the inverter so as to form a latch for the input signal
18 between the inverter and the weakened inverter;
19 wherein the weakened inverter is biased to produce the feedback signal
20 that swings between the high bias voltage, V_H , and the low bias voltage, V_L ; and

21 wherein V_H is slightly higher than a switching threshold of the inverter, and
22 V_L is slightly lower than the switching threshold of the inverter, whereby the
23 feedback signal causes the input signal to reside within a narrow voltage range
24 near the switching threshold of the inverter, thereby making the inverter sensitive
25 to small transitions in the input signal received on the capacitive receiver pad.

1 16. (Original) The means of claim 15, further comprising an amplifying
2 means for amplifying an output of the inverter through an amplification stage to
3 produce an amplified output signal.

1 17-18 (Canceled).

1 19. (Previously presented) The means of claim 16, further comprising an
2 adjusting means for adjusting the high bias voltage generator and the low bias
3 voltage generator to provide a specified sensitivity to transitions of the input
4 signal.

1 20. (Previously presented) The means of claim 16, further comprising an
2 adjusting means for adjusting the high bias voltage generator and the low bias
3 voltage generator to provide a specified noise immunity to noise associated with
4 the input signal.

1 21 (Canceled).

1 22. (New) The method of claim 1, further comprising adjusting an RC time
2 constant for the feedback signal so that the time constant for the feedback signal is
3 significantly larger than the time constant for the transmitted signal from the

4 capacitive transmitter pad, thereby ensuring that the feedback signal does not
5 mask transitions of the transmitted signal.

1 23. (New) The apparatus of claim 8, further comprising an adjusting
2 mechanism configured to adjust an RC time constant for the feedback signal so
3 that the time constant for the feedback signal is significantly larger than the time
4 constant for the transmitted signal from the capacitive transmitter pad, thereby
5 ensuring that the feedback signal does not mask transitions of the transmitted
6 signal.

1 24. (New) The means of claim 15, further comprising an adjusting means
2 for adjusting an RC time constant for the feedback signal so that the time constant
3 for the feedback signal is significantly larger than the time constant for the
4 transmitted signal from the capacitive transmitter pad, thereby ensuring that the
5 feedback signal does not mask transitions of the transmitted signal.